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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,391	07/09/2003	Dong-Jun Kim	SAM-0203DIV	9801

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EXAMINER
BOOTH, RICHARD A

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,391	KIM ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeuch, U.S. Patent 4,851,365.

Jeuch shows the invention as claimed including a method of fabricating a non-volatile semiconductor memory device comprising: forming a charge storage layer 104 on a substrate 100; forming a control gate layer 108 on the charge storage layer; forming a gate mask 118 in the shape of a spacer on the control gate layer; and removing the charge storage layer and the control gate layer, wherein the gate mask 118 protects a portion of the charge storage layer and the control gate layer to form a control gate and a charge storage layer (see figs. 4A-4H and col. 5-line 27 to col. 8-line 52).

Concerning claim 2, note that Jeuch also discloses: forming a disposable pattern 112 on the control gate layer; forming a gate mask layer on the disposable pattern and the control gate layer; and removing a portion of the gate mask layer to form a gate mask 118 on a sidewall of the disposable pattern.

With respect to claim 3, Jeuch also discloses: etching the charge storage layer 104 and the control gate layer 108 using the gate mask and the disposable pattern as a

etching mask thereby protecting a portion of the remaining charge storage layer and the control gate layer under the gate mask and the disposable pattern (see fig. 4F); removing the disposable pattern (see fig. 4e); and etching the remaining portion of the charge storage layer and the control gate layer using the gate mask as an etching mask thereby forming a control gate and a charge storage region under the gate mask.

Regarding claim 8, note that Jeuch discloses: forming a floating gate dielectric layer 102 on the substrate 100; forming a floating gate layer 104 on the floating gate dielectric layer; and forming an inter poly dielectric layer 106 on the floating gate layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeuch, U.S. Patent 4,851,365 in view of Baker et al., U.S. Patent 4,852,062.

Jeuch is applied as above but fails to expressly disclose forming a source-side spacer on the sidewalls of the control gate and the charge storage region; and forming a source electrode on the source, wherein the source electrode is isolated from the control gate and the charge storage region by the source side spacer.

Baker et al. discloses forming a source-side spacer 60 on the sidewalls of the control gate and charge storage region; and forming a source electrode 78 on the

source, wherein the source electrode is isolated from the control gate and the charge storage region by the source side spacer (see Figures 11-12 and col. 7-line 11 to col. 8-line 25). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Jeuch so as to form the source-side spacer and electrode of Baker et al. because this allows for faster programming of the EPROM device (see abstract).

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeuch, U.S. Patent 4,851,365 in view of Lee, U.S. Patent 5,073,513.

Jeuch is applied as above but fails to expressly disclose forming a select gate in the form of a spacer on a sidewall of the charge storage region.

Lee discloses forming a select gate 30 in the form of a spacer on the sidewall of the charge storage region (see fig. 16A and col. 5-line 58 and col. 6-line 26). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Jeuch so as to form a select gate spacer because this eliminates the need for a separate select transistor.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeuch, U.S. Patent 4,851,365 in view of Lee, U.S. Patent 5,073,513 as applied to claim 5 above, and further in view of Chen, U.S. Patent 6,291,297 and Kapoor, U.S. Patent 5,498,558.

Jeuch and Lee are applied as above but fail to expressly disclose forming the LDD region in the substrate using the select gate as an LDD implantation mask; and forming a LDD spacer on a sidewall of the select gate.

Chen discloses forming a select gate 59 on the sidewall of a flash memory cell structure and performing an implant self-aligned to the select gate to form the source/drain region 64 followed by forming a LDD spacer 66 on the select gate (see figs. 4F-4G and col. 5-lines 37-64). While not illustrating a LDD structure, Kapoor discloses the use of an LDD structure in a flash memory device (see col. 6-lines 53-56). In view of these disclosures, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chen so as to perform an implant after the formation of the spacer 66 in order to complete the LDD structure. Furthermore, it also would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Jeuch modified by Lee so as to create a select gate/LDD configuration as suggested by Chen and Kapoor because this is desirable, as suggested by Kapoor, for EPROMs with small channel lengths.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeuch, U.S. Patent 4,851,365 in view of Mitchell et al., U.S. Patent 5,120,672.

Jeuch is applied as above but fails to expressly disclose forming the charge storage layer comprising forming an ONO layer on the substrate.

Mitchell discloses forming an ONO floating gate electrode structure 28 (see fig. 2 and col. 3-line 37 to col. 4-line 10). In view of this disclosure, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Jeuch so as to form the floating gate electrode of ONO as suggested by Mitchell because the ONO structure of Mitchell allows for a high quality memory device which obviates the need for a select gate transistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-1782.

Richard A. Booth
Primary Examiner
Art Unit 2812